CLAIMS AS AMENDED PURSUANT TO 37 CFR 1.121(c)(i)

Replace all claims with the claims shown below. All rejected claims have been canceled.

1. (Previously Presented) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising compounds of gallium and oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

2. (Previously Presented) The transistor of claim 1 wherein said first layer forms an atomically abrupt interface with said upper surface.

3. (Previously Presented) The transistor of claim 1 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element.

4. (Previously Presented) The transistor of claim 3 wherein said gate insulator structure further comprises at a third layer containing gallium and oxygen.

5. (Previously Presented) The transistor of claim 1 said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. (Previously Presented) The transistor of claim 1 wherein said gate insulator structure

has a thickness of 20-300 angstroms.

7. (Previously Presented) The transistor of claim 1 wherein said first layer forms an interface with said upper surface that extend less than four atomic layers in depth of structural interface modulation.

8. (Previously Presented) The transistor of claim 1 wherein said first layer and said gate insulator structure protects said upper surface.

9. (Previously Presented) The transistor of claim 1 wherein said gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

10. (Previously Presented) The transistor of claim 1 wherein said source and drain ion implants provide one of an n-channel or p-channel.

11. (Previously Presented) The transistor of claim 1 wherein said source and drain ion implants comprise at least one of Be/F and C/F.

12. (Previously Presented) The transistor of claim 1 wherein said upper surface comprises GaAs.

13. (Previously Presented) The transistor of claim 1 wherein said upper surface comprises $In_xGa_{1-x}As$.

14. (Previously Presented) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

gate insulator structure on said upper surface, said gate insulator structure comprising a

first layer, a second layer, and a third layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer substantially comprising compounds of gallium and oxygen and at least one rare earth element such that the normalized relative composition of at least one of gallium, oxygen, and said at least one rare earth element in said second layer varies in a monotonic manner as a function of depth within said second insulating layer;

said third layer above said second layer, said third layer substantially comprising gallium oxygen and at least one rare earth element, said third layer being insulating;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

15. (Previously Presented) The transistor of claim 14 wherein said first layer forms an atomically abrupt interface with said upper surface.

16. (Previously Presented) The transistor of claim 14 wherein the gate insulator structure comprises a varying layer that substantially comprises gallium, oxygen, and at least one rare-earth element in which relative concentration of at least one of gallium, oxygen, and said at least one rare earth in said varying layer monotonically vary with depth in said layer.

17. (Previously Presented) The transistor of claim 14 wherein said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

18. (Previously Presented) The transistor of claim 14 wherein the gate insulator structure has a thickness of 20-300 angstroms.

19. (Previously Presented) The transistor of claim 14 wherein said first layer forms an

interface with the compound semiconductor wafer structure that extend less than four atomic layers in depth of modulation of said interface.

20. (Previously Presented) The transistor of claim 14 wherein said first layer and said gate insulator structure protects said upper surface.

21. (Previously Presented) The transistor of claim 14 wherein said gate electrode comprises a metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

22. (Previously Presented) The transistor of claim 14 wherein said source and drain ion implants define an n-channel.

23. (Previously Presented) The transistor of claim 14 wherein said source and drain ion implants comprise and Be/F and C/F, and define a p-channel.

24. (Previously Presented) The transistor of claim 14 wherein said upper surface comprises GaAs.

25. (Previously Presented) The transistor of claim 14 wherein said upper surface comprises $In_xGa_{1-x}As$.

26. (Previously Presented) An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure positioned on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprises gallium, oxygen, and at least one rare-earth element;

a gate electrode positioned on said multilayer gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas; and dielectric spacers positioned on sidewalls of said gate electrode.

27-35. - Canceled by this amendment.

36. Canceled.

37. (Previously presented) A complementary metal-oxide compound semiconductor integrated circuit comprising the transistor of claim 1, 14, or 26 integrated together with similar and complementary transistor devices to form said complementary metal-oxide compound semiconductor integrated circuit.

38. Canceled.

39. (Previously Presented) An enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

40. (Previously Presented) The structure of claim 39 wherein said gate electrode comprises a refractory metal.

41. (Previously Presented) The structure of claim 39 wherein said gate electrode

comprises a member of the group consisting of W, WN, WSi , and combinations thereof.

42. (Previously Presented) The structure of claim 39 wherein said gate insulator structure further comprises a third layer.

43. (Previously Presented) The structure of claim 42 wherein said third layer comprises compounds comprising gallium and oxygen.

44. (Previously Presented) The structure of claim 43 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

45. (Previously Presented) The structure of claim 44 wherein a composition of said third layer varies monotonically with depth in said third layer.

46. (Previously Presented) The structure of claim 43 wherein said gate insulator structure further comprises a fourth layer.

47. (Previously Presented) The structure of claim 43 wherein said fourth layer comprises compounds comprising gallium and oxygen.

48. (Previously Presented) The structure of claim 47 wherein compounds of said fourth layer comprising gallium and oxygen further comprise a rare earth element.

49. (Previously Presented) The structure of claim 39 wherein said first layer is adjacent and in contact with said upper surface.

50. (Previously Presented) The structure of claim 39 further comprising source and drain contacts.

51. (Previously Presented) The structure of claim 39 wherein said source and drain contacts are rapid thermal annealed in UHV.

52. (Previously Presented) The structure of claim 39 wherein said gate insulator structure passivates said upper surface.

53. (Previously Presented) A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

54. (Previously Presented) The method of claim 53 comprising rapid thermal annealing said structure in UHV.

55. (Previously Presented) The method of claim 54 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.

56. Canceled.

57. (Previously Presented) The transistor of claim 14 wherein said upper surface of said compound semiconductor wafer structure is formed from a layer comprising InGaP.

58. (Previously Presented) An enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound including at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

59. (Previously Presented) A method for forming an enhancement mode metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound including at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

60-63. Canceled.

64. (Previously Presented) A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising compounds of gallium and oxygen and at least one rare earth element;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

65. (Previously Presented) The transistor of claim 64 wherein said first layer forms an atomically abrupt interface with said upper surface.

66. (Previously Presented) The transistor of claim 64 wherein said gate insulator structure is composed of at least three layers, including a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element.

67. (Previously Presented) The transistor of claim 66 wherein said gate insulator structure further comprises at a third layer containing gallium and oxygen.

68. (Previously Presented) The transistor of claim 64 said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

69. (Previously Presented) The transistor of claim 64 wherein said gate insulator structure has a thickness of 20-300 angstroms.

70. (Previously Presented) The transistor of claim 64 wherein said first layer forms an interface with said upper surface that extend less than four atomic layers in depth of structural interface modulation.

71. (Previously Presented) The transistor of claim 64 wherein said first layer and said gate insulator structure protects said upper surface.

72. (Previously Presented) The transistor of claim 64 wherein said gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator

structure at 700°C.

73. (Previously Presented) The transistor of claim 64 wherein said source and drain ion implants provide one of an n-channel or p-channel.

74. (Previously Presented) The transistor of claim 64 wherein said source and drain ion implants comprise at least one of Be/F and C/F.

75. (Previously Presented) The transistor of claim 64 wherein said upper surface comprises GaAs.

76. (Previously Presented) The transistor of claim 64 wherein said upper surface comprises $In_xGa_{1-x}As$.

77. (Previously Presented) A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

gate insulator structure on said upper surface, said gate insulator structure comprising a first layer, a second layer, and a third layer;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer substantially comprising compounds of gallium and oxygen and at least one rare earth element such that the normalized relative composition of at least one of gallium, oxygen, and said at least one rare earth element in said second layer varies in a monotonic manner as a function of depth within said second insulating layer;

said third layer above said second layer, said third layer substantially comprising gallium oxygen and at least one rare earth element, said third layer being insulating;

a gate electrode positioned on said gate insulator structure;

source and drain ion implants self-aligned to said gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein said gate electrode comprises a metal selected from the group consisting of W, WN, WSi , and combinations thereof.

78. (Previously Presented) The transistor of claim 77 wherein said first layer forms an atomically abrupt interface with said upper surface.

79. (Previously Presented) The transistor of claim 77 wherein the gate insulator structure comprises a varying layer that substantially comprises gallium, oxygen, and at least one rare-earth element in which relative concentration of at least one of gallium, oxygen, and said at least one rare earth in said varying layer monotonically vary with depth in said layer.

80. (Previously Presented) The transistor of claim 77 wherein said first layer has a thickness of more than 10 angstroms and less than 25 angstroms.

81. (Previously Presented) The transistor of claim 77 wherein the gate insulator structure has a thickness of 20-300 angstroms.

82. (Previously Presented) The transistor of claim 77 wherein said first layer forms an interface with the compound semiconductor wafer structure that extend less than four atomic layers in depth of modulation of said interface.

83. (Previously Presented) The transistor of claim 77 wherein said first layer and said gate insulator structure protects said upper surface.

84. (Previously Presented) The transistor of claim 77 wherein said gate electrode comprises a metal which is stable in presence of the top layer of the gate insulator structure at 700°C.

85. (Previously Presented) The transistor of claim 77 wherein said source and drain ion

implants define an n-channel.

86. (Previously Presented) The transistor of claim 77 wherein said source and drain ion implants comprise and Be/F and C/F, and define a p-channel.

87. (Previously Presented) The transistor of claim 77 wherein said upper surface comprises GaAs.

88. (Previously Presented) The transistor of claim 77 wherein said upper surface comprises $In_xGa_{1-x}As$.

89. (Previously Presented) A metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure positioned on said upper surface, said multilayer gate insulator structure substantially comprising alternating layers each of which comprises gallium, oxygen, and at least one rare-earth element;

a gate electrode positioned on said multilayer gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

and dielectric spacers positioned on sidewalls of said gate electrode.

90. Canceled.

91. (Previously Presented) A complementary metal-oxide compound semiconductor integrated circuit comprising the transistor of claim 64, 77, or 89 integrated together with similar and complementary transistor devices to form said complementary metal-oxide compound semiconductor integrated circuit.

92. Canceled.

93. (Previously Presented) A metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

94. (Previously Presented) The structure of claim 93 wherein said gate electrode comprises a refractory metal.

95. (Previously Presented) The structure of claim 93 wherein said gate electrode comprises a member of the group consisting of W, WN, WSi , and combinations thereof.

96. (Previously Presented) The structure of claim 93 wherein said gate insulator structure further comprises a third layer.

97. (Previously Presented) The structure of claim 96 wherein said third layer comprises compounds comprising gallium and oxygen.

98. (Previously Presented) The structure of claim 97 wherein compounds of said third layer comprising gallium and oxygen further comprise a rare earth element.

99. (Previously Presented) The structure of claim 98 wherein a composition of said third layer varies monotonically with depth in said third layer.

100. (Previously Presented) The structure of claim 97 wherein said gate insulator structure further comprises a fourth layer.

101. (Previously Presented) The structure of claim 97 wherein said fourth layer comprises compounds comprising gallium and oxygen.

102. (Previously Presented) The structure of claim 101 wherein compounds of said fourth layer comprising gallium and oxygen further comprise a rare earth element.

103. (Previously Presented) The structure of claim 93 wherein said first layer is adjacent and in contact with said upper surface.

104. (Previously Presented) The structure of claim 93 further comprising source and drain contacts.

105. (Previously Presented) The structure of claim 93 wherein said source and drain contacts are rapid thermal annealed in UHV.

106. (Previously Presented) The structure of claim 93 wherein said gate insulator structure passivates said upper surface.

107. (Previously Presented) A method for forming a metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound of gallium, oxygen and at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

108. (Previously Presented) The method of claim 107 comprising rapid thermal annealing said structure in UHV.

109. (Previously Presented) The method of claim 108 wherein said rapid thermal annealing comprising annealing at between 700 and 900 degrees Centigrade.

110. Canceled..

111. (Previously Presented) The transistor of claim 77 wherein said upper surface of said compound semiconductor wafer structure is formed from a layer comprising InGaP.

112. (Previously Presented) A metal-oxide-compound semiconductor field effect transistor structure, comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure comprising a first layer and a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound including at least one rare earth element; and

a gate electrode positioned on said gate insulator structure.

113. (Previously Presented) A method for forming a metal-oxide-compound semiconductor field effect transistor structure, comprising:

providing a compound semiconductor wafer structure having an upper surface;

depositing a gate insulator structure comprising depositing a first layer and depositing a second layer, said gate insulator on said upper surface;

said first layer substantially comprising compounds of gallium and oxygen;

said second layer comprising at least one compound including at least one rare earth element; and

depositing a gate electrode positioned on said gate insulator structure.

114-117. Canceled.

118. (Previously Presented) The transistor of any one of claims 64, 77, and 89 wherein said transistor defines a depletion mode transistor.

119. (Previously Presented) A compound semiconductor structure comprising:

a GaAs-based supporting semiconductor structure;

a first layer of gallium oxide located on a surface of the supporting semiconductor structure to form an interface therewith; and

a second layer of a Ga--Gd oxide disposed on the first layer.

120. (Previously Presented) The compound semiconductor structure of claim 119 wherein the Ga--Gd oxide is Gd3Ga5O12.

121. (Previously Presented) The compound semiconductor structure of claim 119 wherein the GaAs-based supporting semiconductor structure is a GaAs-based heterostructure.

122. (Previously Presented) The compound semiconductor structure of claim 121 wherein the GaAs-based supporting semiconductor structure is an at least partially completed metal-oxide field effect transistor.

123-124. Canceled.

125. (Previously Presented) The compound semiconductor structure of claim 119 wherein the first layer of gallium-oxide has a thickness in a range of approximately 0.5 nm to 10

nm.

126. (Previously Presented) The compound semiconductor structure of claim 119 wherein the second layer of Ga--Gd oxide has a thickness in a range of approximately 5 nm to 20 nm.

127. (Previously Presented) A method of forming a dielectric layer structure on a supporting semiconductor structure comprising the steps of:

providing a GaAs-based supporting semiconductor structure;

depositing a first layer of gallium oxide on a surface of the supporting structure; and

depositing a second layer of a Ga--Gd-oxide on the first layer.

128. (Previously Presented) The method of claim 127 wherein the step of depositing the layer of gallium oxide includes depositing the layer of gallium oxide by evaporation.

129. (Previously Presented) The method of claim 128 wherein the step of depositing a layer of gallium oxide on the surface of the supporting semiconductor structure by evaporation includes one of thermal evaporation, electron beam evaporation, and laser ablation.

130. (Previously Presented) The method of claim 129 further comprising the step of evaporating atomic oxygen during at least a portion of the step of depositing the layer of gallium oxide.

131. (Previously Presented) The method of claim 130 where in the step of evaporating atomic oxygen begins after at least one monolayer of gallium oxide has been deposited onto the surface of the supporting semiconductor structure.

132. (Previously Presented) The method of claim 128 wherein the step of depositing the second layer includes the step of evaporating Gd.

133. (Previously Presented) The method of claim 131 wherein the step of depositing the second layer includes the step of evaporating Gd.

134. (Previously Presented) The method of claim 133 wherein the step of evaporating atomic oxygen commences before the step of evaporating Gd.

135. Canceled.

136. (Previously Presented) The method of claim 127 wherein the Ga--Gd oxide is Gd.sub.3Ga.sub.5O.sub.12.

137. (Previously Presented) The method of claim 127 wherein the GaAs-based supporting semiconductor structure is a GaAs-based heterostructure.

138. (Previously Presented) The method of claim 137 wherein the GaAs-based supporting semiconductor structure is an at least partially completed metal-oxide field effect transistor.

139-140. Canceled.

141. (Previously Presented) The method of claim 127 wherein the first layer of gallium oxide has a thickness in a range of approximately 0.5 nm to 10 nm.

142. (Previously Presented) The method of claim 127 wherein the second layer of Ga--Gd oxide has a thickness in a range of approximately 5 nm to 20 nm.